What is claimed is:

1. A memory controller comprising:

a state generator configured to generate a plurality of state information signals in response to command requests associated with a plurality of banks in a memory;

an enable signal generator configured to generate a plurality of enable signals indicating whether the state information signals are valid or invalid; and

a bank controller configured to generate a command based on the state information signals and the enable signals.

2. The memory controller of claim 1, wherein the state generator comprises:

a first state generator configured to generate a first state information signal which is one of the state information signals and a first next-cycle state information signal indicating a state of the first state information signal after a lapse of one clock cycle; and

a second state generator configured to generate a second state information signal which is one of the state information signals and a second next-cycle state information signal indicating a state of the second state information signal after a lapse of one clock cycle.

3. The memory controller of claim 2, further comprising a demultiplexer configured to supply a first command request and a second command request to the first state generator and the second state generator as the command requests associated with the banks, respectively.

4. The memory controller of claim 3, wherein the first state generator comprises:

a first state machine configured to generate the first next-cycle state information signal based on the first command request and the first state information signal; and

a first state register configured to latch the first next-cycle state information signal and to supply the first state information signal to the bank controller.

5. The memory controller of claim 3, wherein the second state generator comprises:

a second state machine configured to generate the second next-cycle state information signal based on the second command request and the second state information signal; and

a second state register configured to latch the second next-cycle state information signal and to supply the second state information signal to the bank controller.

6. The memory controller of claim 2, wherein the enable signal generator comprises:

a first enable signal generator configured to generate a first enable signal which is one of the enable signals, based on the first next-cycle state information signal and the second next-cycle state information signal; and

a second enable signal generator configured to generate a second enable signal which is one of the enable signals, based on the first next-cycle state information signal and the second next-cycle state information signal.

7. The memory controller of claim 6, wherein the first enable signal generator comprises:

a first decision circuit configured to assign a priority to one of the first next-cycle state information signal and the second next-cycle state information signal and to generate a first next-cycle enable signal; and

a first enable register configured to latch the first next-cycle enable signal and to supply the first enable signal to the bank controller.

8. The memory controller of claim 6, wherein the second enable signal generator comprises:

a second decision circuit configured to assign a priority to one of the first next-cycle state information signal and the second next-cycle state information signal and to generate a second next-cycle enable signal; and

a second enable register configured to latch the second next-cycle enable signal and to supply the second enable signal to the bank controller.

9. The memory controller of claim 2, wherein the state generator further comprising:

a third state generator configured to generate a third state information signal which is one of the state information signals and a third next-cycle state information signal indicating a state of the third state information signal after a lapse of one clock cycle; and

a fourth state generator configured to generate a fourth state information signal which is one of the state information signals and a fourth next-cycle state information signal indicating the state of the fourth state information signal after a lapse of one clock cycle.

10. The memory controller of claim 9, further comprising a demultiplexer configured to supply first to fourth command requests to the first to fourth state generators as the command requests associated with the banks, respectively.

11. The memory controller of claim 10, wherein the third state generator comprises:

a third state machine configured to generate the third next-cycle state information signal based on the third command request and the third state information signal; and

a third state register configured to latch the third next-cycle state information signal and to supply the third state information signal to the bank controller.

12. The memory controller of claim 10, wherein the fourth state generator comprises:

a fourth state machine configured to generate the fourth next-cycle state information signal based on the fourth command request and the fourth state information signal; and

a fourth state register configured to latch the fourth next-cycle state information signal and to supply the fourth state information signal to the bank controller.

13. The memory controller of claim 9, wherein the enable signal generator comprises:

a first enable signal generator configured to generate the first enable signal based on the first to fourth next-cycle state information signals;

a second enable signal generator configured to generate the second enable signal based on the first to fourth next-cycle state information signals;

a third enable signal generator configured to generate the third enable signal based on the first to fourth next-cycle state information signals; and

a fourth enable signal generator configured to generate the fourth enable signal based on the first to fourth next-cycle state information signals.

14. The memory controller of claim 13, wherein the first enable signal generator comprises:

a first decision circuit configured to assign a priority to the first to fourth next-cycle state information signals and to generate a first next-cycle enable signal; and

a first enable register configured to latch the first next-cycle enable signal and to supply the first enable signal to the bank controller.

15. The memory controller of claim 13, wherein the second enable signal generator comprises:

a second decision circuit configured to assign a priority to the first to fourth next-cycle state information signals and to generate a second next-cycle enable signal; and

a second enable register configured to latch the second next-cycle enable signal and to supply the second enable signal to the bank controller.

16. The memory controller of claim 13, wherein the third enable signal generator comprises:

a third decision circuit configured to assign a priority to the first to fourth next-cycle state information signals and to generate a third next-cycle enable signal; and

a third enable register configured to latch the third next-cycle enable signal and to supply the third enable signal to the bank controller.

17. The memory controller of claim 13, wherein the fourth enable signal generator comprises:

a fourth decision circuit configured to assign a priority to the first to fourth next-cycle state information signals and to generate a fourth next-cycle enable signal; and

a fourth enable register configured to latch the fourth next-cycle enable signal and to supply the fourth enable signal to the bank controller.

18. A semiconductor integrated circuit comprising:

a memory controller integrated on a semiconductor chip and configured to control a memory by generating a plurality of state information signals and a plurality of enable signals indicating whether the state information signals are valid or invalid, in response to command requests associated with a plurality of banks in the memory; and

a signal processor integrated on the semiconductor chip and configured to perform signal processing and to transmit the command requests to the memory controller.

19. The semiconductor integrated circuit of claim 18, wherein the memory controller comprises:

a state generator configured to generate the state information signals;

an enable signal generator configured to generate the enable signals; and

a bank controller configured to generate a command based on the state information signals and the enable signals.

20. A method for controlling a memory comprising:

generating a plurality of state information signals in response to command requests associated with a plurality of banks in a memory;

generating a plurality of enable signals indicating whether the state information signals are valid or invalid; and

generating a command based on the state information signals and the enable signals.